

MUHAMMAD HAISAM NADEEM

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EDUCATION

University of Manchester - BEng Electrical and Electronic Engineering | September 2024 – Present

Average Grade: 70.5%

Relevant Courses: Computer Systems Architecture, Concurrent Systems, Data Networking, High-Speed Digital & Mixed-Signal Design, Digital Signal Processing, Microcontroller Engineering, Digital System Design, C Programming, Control Systems II, Sensors & Instrumentation

Loreto Sixth Form College - A-Level Mathematics, Biology and Chemistry | 2020 – 2022

EXPERIENCE

Dukosi — ASIC/Digital Engineering Intern

Edinburgh, UK | June 2026 – August 2026

- Worked within the ASIC Digital Engineering team on RTL verification and power analysis of a digital signal processing core.
- Used Cadence Joules to perform RTL power analysis across multiple DSP test cases, identifying key power-consuming logic and applying power-optimization techniques including clock gating to evaluate their impact on power consumption.
- Developed parameterised System Verilog test case and analysed simulation waveforms to investigate digital logic behaviour and switching activity.
- Designed and implemented a **2-way set-associative cache in System Verilog**, incorporating an AMBA APB interface, LRU replacement, write-through behaviour and error handling.
- Developed a System Verilog testbench and APB memory model to verify cache hits, misses, read/write operations and bus error conditions.
- Documented technical workflows and results and presented findings to the ASIC Digital Engineering team.

Technical Projects

Brake System Plausibility Device (BSPD) Design

October 2025

- Designed a Brake System Plausibility Device (BSPD) circuit in KiCad in compliance with Formula Student UK (FSUK) safety regulations, ensuring the system detects simultaneous brake and throttle activation and disconnects power to the motor to protect the driver and vehicle.
- Integrated brake pressure and throttle position sensors into the circuit and monitored their outputs using LM393 comparators, setting threshold levels according to FSUK requirements using a voltage divider network connected to the comparators input and triggering a shutdown relay when unsafe conditions were detected.
- Implemented an RC timing network to meet FSUK-defined delay conditions, ensuring the circuit distinguishes between accidental and sustained simultaneous brake–throttle activation.
- Biased a 2SD1047 transistor to drive the shutdown safety relay, incorporating flyback protection using a 1N4001 diode to a safe relay operation.

Autonomous Buggy

October 2024 – November 2024

- Developed an autonomous Arduino-based vehicle using C++ with ultrasonic obstacle detection.
- Integrated an HC-SR04 ultrasonic sensor, servo motor and L298N motor driver.
- Implemented obstacle-avoidance algorithms using sensor feedback, PWM motor control, conditional logic and loops.
- Debugged and optimised the embedded software to improve navigation reliability.

I/O Board Soldering and Assembly Programming

January 2025 – February 2025

- Assembled and soldered a PCB-based I/O board and interfaced it with a PIC18F8722 microcontroller.
- Developed Assembly programs implementing arithmetic operations and multiplexed 7-segment displays using registers, branching, bit manipulation and subroutines.
- Debugged hardware/software integration using schematics, a multimeter and oscilloscope.

ACTIVITIES & LEADERSHIP

Tutoring - *Engineering Mathematics*
Robotic Society Member

SKILLS

Programming: C, C++, Python, System Verilog, VHDL, Assembly

Hardware / Embedded: STM32 Nucleo-F401RE, PIC18F8722, Arduino, RTL Design, Digital Logic, AMBA APB

Tools: Cadence Joules, Xilinx/Vivado, MPLAB X IDE, KiCad, PLECS, Ansys, Linux, IPSA Power Analysis, VS Code

Laboratory: Oscilloscope, Digital Multimeter, Soldering

LANGUAGES

English (native), Urdu (native), Hindi (fluent), Punjabi (fluent)